REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Claims 1, 11, 15, 19, 21, 25, 28, 30, and 32 have been amended. Claims 41-48 have been added. All the amendments and new claims are supported throughout the specification, for example at paragraphs 11-18 and Figures 2A-2C. No new matter is being added. Thus, upon entry of this reply, claims 1-48 will remain in the application.

Claim rejections - 35 U.S.C. § 112

Claim 11, and its dependent claims 12-14 and 34, were rejected under 35 U.S.C. § 112 as being allegedly indefinite and lacking antecedent basis for the term "the state" in claim 11. Applicants have amended claim 11 to recite "a state" rather than "the state." Accordingly, claims 11-14 and 34 are believed to be sufficiently definite under 35 U.S.C. § 112.

Claim rejections - 35 U.S.C. § 102 and § 103

Claims 1-6, 11-13, 15-16, 32, and 40 were rejected as being allegedly anticipated under 35 U.S.C. § 102 by U.S. Patent No. 6,470,437 to Lyon ("Lyon patent" or "Lyon"). Claims 7-10, 14, 17-31, and 33-39 were rejected as being allegedly obvious under 35 U.S.C. § 103 in light of Lyon.

Applicants teach a technique for extending the local memory address space of a processor. In an embodiment, a processor may include a local addressable memory, such as an SRAM, in parallel with L1 local cache. A local memory controller may examine a local memory descriptor to determine whether a page containing a requested memory location is in the local addressable memory.

If the requested memory location is not in the local addressable memory, the local memory controller may route the access to the local cache instead.

In contrast, Lyon discusses the internal design of a cache itself. Indeed, each of the figures in Lyon are diagrams of different cache architecture designs. Lyon does not disclose the design of a structure external to a cache.

All of the section 102 and 103 rejections in the Office Action are predicated on equating the local addressable memory to a cache or to structures within a cache. Independent claims 1, 11, 15, 19, 21, 25, 28, 30, and 32 have been amended, and new claims 41-48 have been added, to further clarify that the local addressable memory is not a cache and it is not equivalent to structures within a cache.

For example, claim 1 now recites, *inter alia*, "wherein a portion of a system memory is mapped to the local addressable memory." This is in marked contrast to a cache, which is not mapped to by any portion of system memory. A cache only holds temporary copies of data from a real memory location; it is the real memory location that is mapped to by the system memory, not the cache. In the claimed subject matter, however, a portion of system memory is mapped to the local addressable memory itself.

Accordingly, the claimed subject matter is significantly different from the cache designs discussed by Lyon. Applicants respectfully submit that claims 1-48, as amended, are not anticipated or made obvious by Lyon.

Conclusion

Applicants ask that all claims be allowed. Please apply all applicable charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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/BY BING AI REG. NO. 43,312

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